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A New Pedagogical Approach for Solid State Electronic Device Education: the Variational Thermodynamic Technique for Modeling

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A New Pedagogical Approach for Solid State Electronic Device Education: the Variational Thermodynamic Technique for Modeling

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Unquestionably, one of the most important developments in this century has been the avalanche advancement of solid state device technology into physical regions never before imagined possible. The attendant consequences for economies around the globe has propelled Science Technology Engineering and Mathematics (STEM) teaching to top levels of concern among politicians and urgent course demand among budding would-be engineers. Unfortunately, even the rudiments of the subject need grounding in what used to be advanced physics: many lose heart at the mysteries of quantum mechanics and the subtleties of new transistor architectures.

We have developed and here apply a methodology capable of modeling the internal workings of a Trench Insulated-Gate Bipolar Transistor (TIGBT) which applications information is given in Fig. 1 and internal structure is given in Fig. 2. The TIGBT is a relatively new transistor design which lies at the heart of many power electronics applications in areas such as smart grids, renewable energy, and hybrid electric vehicles, etc. [1].

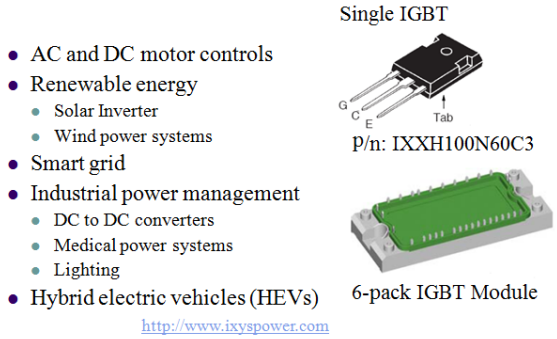


Figure 1: TIGBT and its applications

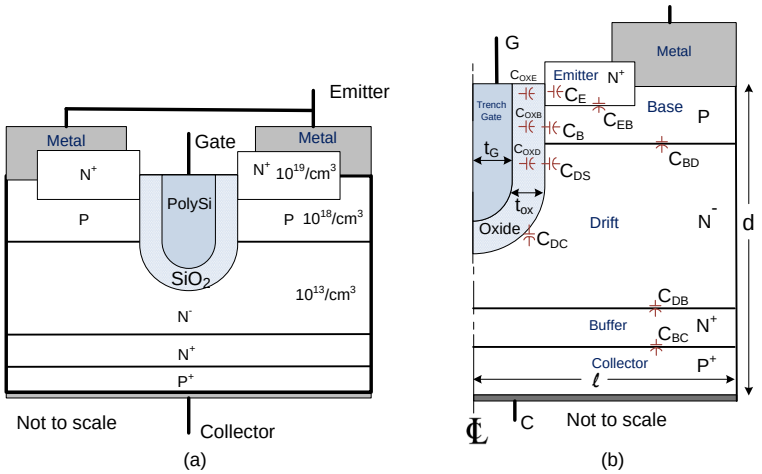


Figure 2: (a) Schematic of the cross-section of a cell of the Trench-Gated IGBT structure showing different active layers including typical doping levels of silicon regions. (b) cross section of a symmetric half-cell TIGBT indicating capacitances and dimensional parameters, typically t_{ox}=1000 Å, ℓ = 10 µm, d = 100 µm, t_G = 1 µm.

Our method consists of finding trial functions for the interior distribution of electrical potential and which cause the Helmholtz Free Energy of the entire device to be minimum. We posit these trial functions in the various electrically active regions of the transistor. The trial functions are chosen to be continuous and locally to solve Poisson's equation. We imbed parameters in them so that when the free energy functional is evaluated it becomes a *function* of the parameters. We then minimize the Free Energy using the trial function parameters [3-8].

The VT methodology flow is given in Fig. 3. This process is really very simple, but for those unexposed to the 'direct method' of variational minimization it can sound vague and be confusing unless accompanied by concrete examples. Consider the sub-region of the TIGBT which consists of the p-Si substrate, the adjacent oxide layer, and the portion of the gate adjacent to this. The trial function within the gate is assumed to be a simple constant axially and radially.

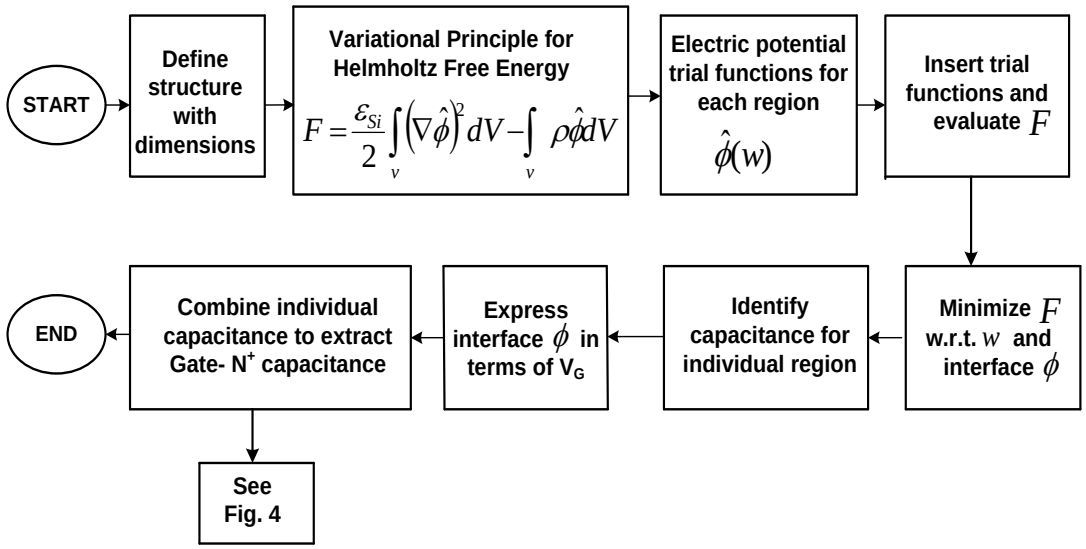
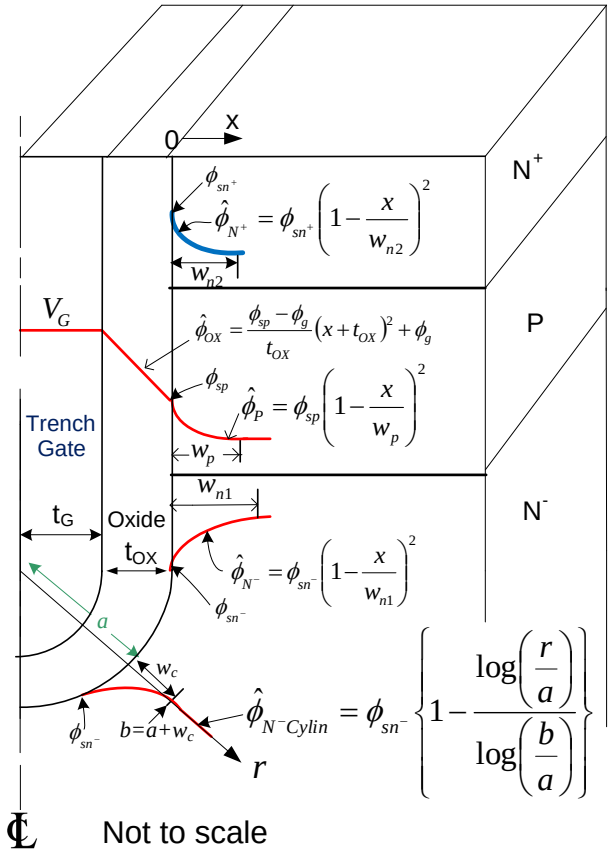


Figure 3: Variational Thermodynamic Methodology flow for obtaining MOS structure capacitance

In this paper a trial function is designated by bearing a hat. Figure 4 gives a complete account of the trial functions which we used in this analysis. The trial function within the oxide is taken to be a linear variation between the gate potential, V_G, and the interface potential, ϕ_{sp}, of the p-Si. Although, in reality this potential distribution is three-dimensional we ignore all variations except in the x-direction. We choose the trial function in the p-Si to be a simple quadratic form as follows:

$$\hat{\phi}_P(x) = \phi_{sp}\left(1 - \frac{x}{w_p}\right)^2 \qquad (1)$$



$\hat{\phi}_{N^+}$ = N $^+$ potential trial function
$\hat{\phi}_G$ = Gate potential trial function
ϕ_G = Gate potential
$\hat{\phi}_{OX}$ = Oxide potential trial function
ϕ_{sp} = P base - oxide interface potential
$\hat{\phi}_P$ = P potential trial function
$\hat{\phi}_{N^-}$ = N $^-$ potential trial function
$\hat{\phi}_{N^-cylin}$ = N $^-$ potential trial function near gate tip
ϕ_{sn+} = N$^+$ region-oxide interface potential
ϕ_{sn-} = N $^-$ drift-oxide interface potential
t_G = Half- cell Trench Gate thickness
t_{OX} = Gate oxide thickness
w_p = P depletion layer thickness
w_{n1} = N $^-$ depletion layer thickness
w_c = N $^-$ depletion layer thickness near gate tip
w_{n2} = N $^+$ depletion layer thickness
r = Radial distance from the cylindrical axis

Figure 4: Showing half-cell with potential 'trial functions' for the Gate, Oxide, P, N$^+$, and N$^-$ regions, respectively.

With proper choice of w_p, this function will locally solve Poisson's equation in one-dimension. Our view point is thermodynamic, rather than solving differential equations, however, and so we insert this trial function into the free energy functional and evaluate the total energy F [4-5].

For this discussion, we shall show the first few steps in the process of treating the p-Si region. This region is connected to ground at some point where $x >> w_p$, and so the trial function will be zero for $x \geq w_p$. In advanced treatices of the thermodynamic of phase change, w_p, is the 'correlation distance', while ϕ_s is the 'order parameter' [3].

Inserting $\hat{\phi}_p(x)$ into the free energy functional we get:

$$F = \frac{\varepsilon}{2}\int_v |\nabla\phi|^2 dV - \int_v \rho\phi dV$$

$$= \frac{2}{3}\frac{\varepsilon_{si}}{w_p}\phi_s^2 + \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\left(V_g - \phi_s\right)^2 + \frac{1}{3}qN_A w_p \phi_s \qquad (2)$$

Both the parameters w_p and ϕ_s are internal and must be determined by minimizing the expression above.

Thus, we must have

$$\frac{\partial F_p}{\partial w_p} = -\frac{2}{3}\frac{\varepsilon_{si}}{w_p^2}\phi_s^2 + \frac{1}{3}qN_A\phi_s = 0$$

Which implies,

$$w_p^2 = \frac{2\varepsilon_{si}\phi_s}{qN_A} \qquad (3)$$

And now, insert these results into equation (2) to get the free energy as a function of (the still undetermined) ϕ_{sp},

$$F_p = \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}}\left(V_g - \phi_s\right)^2 + \frac{2}{3}\sqrt{2\varepsilon_{si}qN_A}\phi_s^{3/2} \qquad (4)$$

The parameter ϕ_{sp} is determined by using the condition $\frac{\partial F_p}{\partial \phi_s} = 0$

This gives us

$$\left(\frac{\varepsilon_{ox}}{t_{ox}}\right)^2\left(V_g - \phi_s\right)^2 - 2\varepsilon_{si}qN_A\phi_s = 0 \qquad (5)$$

Thus, we get ϕ_{sp} in a simple closed form expression which involves only the known quantities V_G, N_A, ε_{si}, and t_{ox}. The expression above is a quadratic equation in ϕ_{sp}, so it has two branches of solution, one for negative applied bias and one for positive applied bias [4-5].

We plot the result in Fig. 5 for each of these substrate layers as a function of applied gate voltage. We also plot the w parameters for each region against their respective interface potential, ϕ_s, shown in Fig. 6. These plots include the effect of mobile charge. Mobile charge effects are very important but cannot be discussed adequately here.

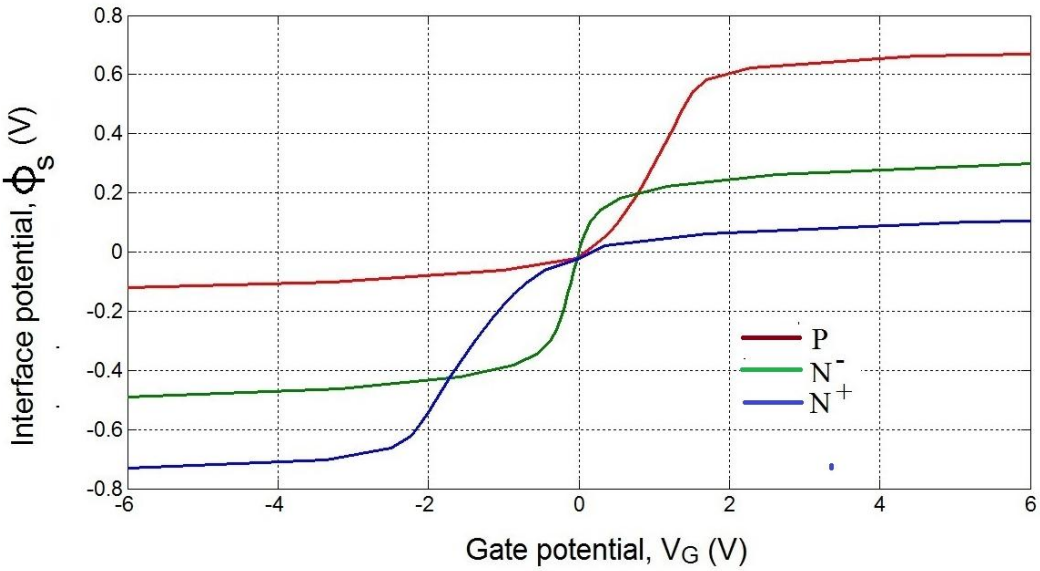


Figure 5: Interface potential (Φ_S) vs. gate potential (V_G) for P (Red), N^- (Green), and N^+ (Blue) regions.

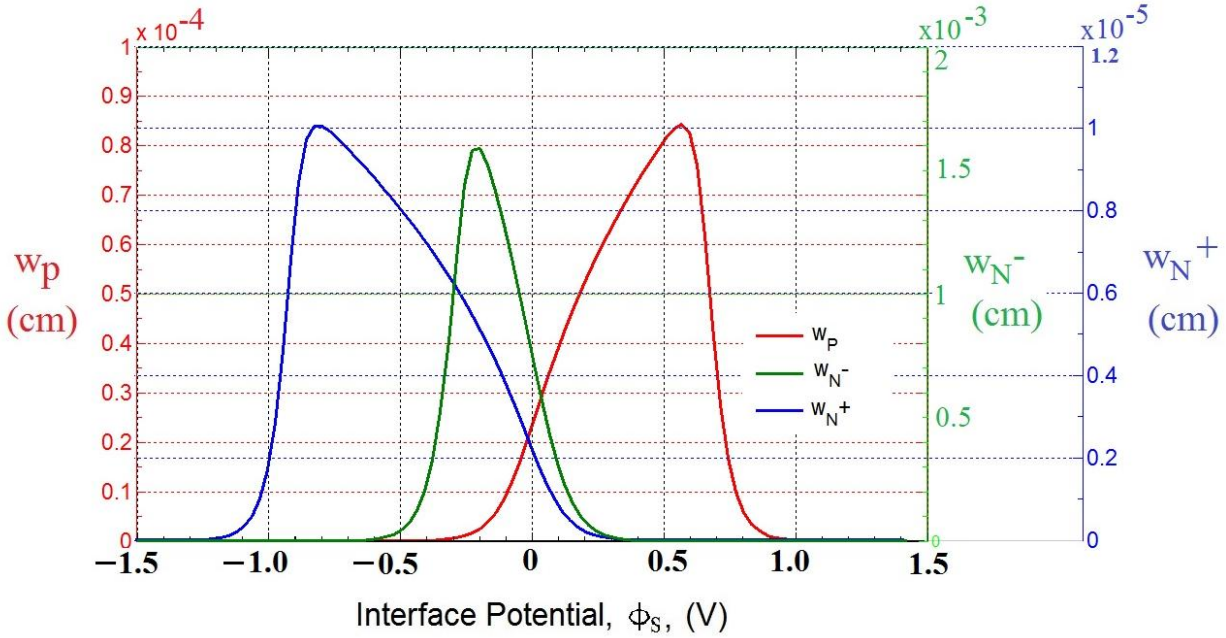


Figure 6: Relaxation distance (w) vs. interface potential (Φ_S) of P (Red), N^- (Green), and N^+ (Blue) regions.

Thus, our approach gives complete and exact agreement with the one-dimensional discussion found in text books where only depletion approximation (DA) is used [2]. In addition our method can be readily extended to include mobile charge; albeit at the expense of considerable mathematical complexity needed to accommodate Fermi-Dirac statistics.

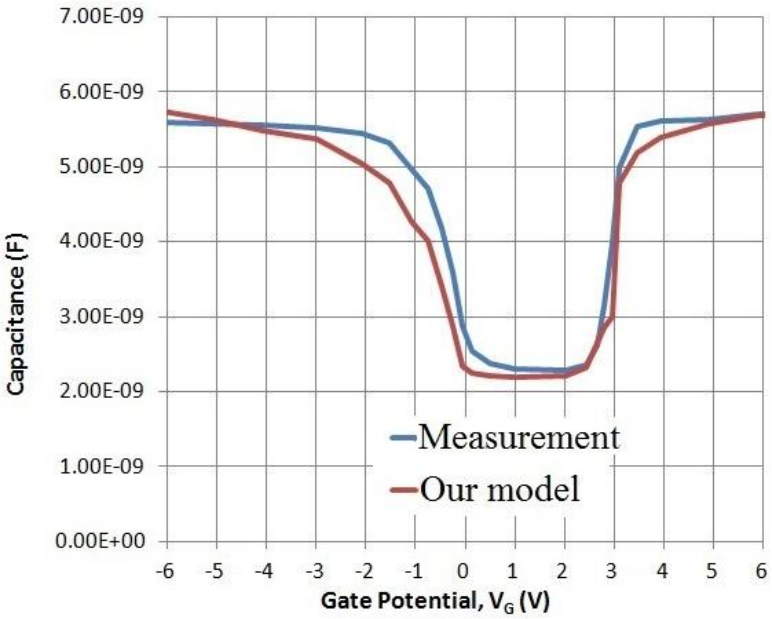


Figure 7: Measured gate-to- emitter capacitance (Blue) and our model (Red).

The final result of these efforts is shown in Fig. 7, where we compare our model result for the C-V characteristics with that measured in our laboratory using Keithley Model 4200-SCS Semiconductor Characterization System. Note that the C-V shows that the device is essentially closed electrically to the outside world, except for a narrow window close to V_G =0, where it presents a small uniform capacitance in response to the gate bias. These are good qualities for a power transistor to have. In summary, our VT approach is easy to understand; thoroughly physics based and can be implemented using commonly available hardware and software.

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